## REMARKS

In view of the above amendments and the following remarks, reconsideration of the objections and rejections set forth in the Office Action of December 29, 2005 is respectfully requested.

In order to make necessary editorial corrections, the entire specification and abstract have been reviewed and revised. As the revisions are quite extensive, the amendments to the specification and abstract have been incorporated into the attached substitute specification and abstract. For the Examiner's benefit, a marked-up copy of the specification indicating the changes made thereto is also enclosed. No new matter has been added by the revisions. Entry of the substitute specification is thus respectfully requested.

The Examiner objected to the drawings as not showing all of the elements described in the specification. In particular, the Examiner asserted that element 122 identified on page 17 of the original specification was not illustrated in figure 29 as indicated in the specification. However, the Examiner is requested to note that the reference to element "122" on page 17, line 17 of the original specification was a typographical error, and should have read "192" (indicating the X, Y table in figure 29). Thus, upon reviewing the specification as explained above, the typographical error on page 17 of the original specification was also corrected. Therefore, it is submitted that the Examiner's objection to the drawings has been overcome.

The Examiner rejected claims 1-15 as being unpatentable over the Shibata reference (USP 6,193,132) in view of the Nishimaki reference (USP 5,566,876). However, the original claims have now been cancelled and replaced with new claims 16-32 as indicated above. For the reasons discussed below, it is respectfully submitted that the new claims are clearly patentable over the prior art of record.

New independent claim 16 is directed to a method of correcting inclination of ICs on a semiconductor wafer, comprising correcting inclination of all the ICs on the semiconductor wafer with respect to an X axis and Y axis by *rotating the semiconductor wafer in a circumferential direction thereof using a wafer turning member* based on the result of recognizing a first detection point and a second detection point on the semiconductor wafer. Similarly, new

independent claim 24 is directed to an apparatus that comprises a wafer turning member on which a semiconductor wafer is to be loaded, and the wafer turning member is operable *to rotate the semiconductor wafer in a circumferential direction thereof.* The apparatus further comprises a control device for controlling a turning device for turning the wafer turning member, and the controlling of the turning device is based on inclination information of the ICs detected by a recognition device *so as to rotate the semiconductor wafer loaded on the wafer turning member to thereby correct the inclination of all of the ICs on the semiconductor wafer.*

Thus, as recited in both new independent claim 16 and new independent claim 24, the *semiconductor wafer is rotated* in a circumferential direction thereof so as to correct the inclination of all the ICs on the semiconductor wafer with respect to an X-axis and a Y-axis. Therefore, as explained on page 8, lines 1-6 of the original specification, the process of correcting the inclination of the ICs on the semiconductor wafer is simplified so as to allow improved productivity.

The Shibata reference is directed to a method of bonding a semiconductor chip. However, as acknowledged by the Examiner on page 4 of the Office Action, the Shibata reference does not disclose or even suggest correction of an inclination of all ICs on a semiconductor wafer. Nonetheless, the Examiner asserted that the Nishimaki reference discloses this feature. As will be explained in detail below, the Applicants respectfully disagree with the Examiner's assertion.

The Nishimaki reference is directed to a wire bonder and wire bonding method, in which an IC chip 6 is supported on a bonding stage 7. A camera 1 and a bonding head 3 are connected to an X-Y table so that the X-Y table can move the camera 1 and the bonding head 3 as necessary (see column 4, lines 46-49 of the Nishimaki reference). In the Office Action, the Examiner asserted that the Nishimaki reference also discloses turning a semiconductor wafer so as to correct individual bonding reference coordinates so that a bonding site agrees with a proper bonding site (see page 5, lines 5-9 of the Office Action). However, the Examiner appears to be misunderstanding the Nishimaki reference.

Firstly, the Examiner referred to column 9, lines 44-46; and column 12, lines 35-46 as providing support for the Examiner's assertion that the semiconductor wafer of the Nishimaki reference is turned. However, column 9, lines 44-66 describes the *calculation of a corrected bonding position* using the difference between reference position data stored in the memory prior to the bonding procedure and newly-acquired image information of the actual position of a lead 20. Column 12, lines 35-46 of the Nishimaki reference also describes the calculation of a corrected bonding position. Both of these sections of the Nishimaki reference also teach that positional corrections are made based on the calculations described above. However, the Nishimaki reference does not disclose or suggest *moving (e.g., rotating) the semiconductor wafer* so as to obtain these positional corrections. In contrast, as explained above, the X-Y table 4 moves *the bonding head 3 and the camera 1*, rather than the bonding stage 7 supporting a wafer, in order to achieve the positional corrections. In other words, the positional corrections calculated as described in column 9, lines 44-66 and column 12, lines 35-46 of the Nishimaki reference are used to *adjust the position of the bonding head 3 and the camera 1* (see column 8, lines 56-62). The Nishimaki reference does not, however, disclose or even suggest even moving a semiconductor wafer to correct an inclination (i.e., a position) of ICs on a semiconductor wafer.

Secondly, the Nishimaki reference teaches that a lead frame (i.e., semiconductor wafer) is transported in a generally linear direction by a pair of guide rails 30, 31(see column 5, lines 29 through column 7, line 20) so as, for example, to be loaded onto the bonding stage 7. However, the Nishimaki reference does not disclose or even suggest *rotating* a semiconductor wafer in a circumferential direction of the semiconductor wafer, or a device for rotating the semiconductor wafer in a circumferential direction thereof. Thus, the Nishimaki reference also does not disclose or suggest rotating the semiconductor wafer so as to correct the inclination of the ICs on the semiconductor wafer.

As explained above, the Nishimaki reference does not disclose or even suggest moving a semiconductor wafer so as to correct inclination of ICs on the semiconductor wafer. Moreover, the Nishimaki reference does not disclose or even suggest *rotating* the semiconductor wafer. Therefore, one of ordinary skill in the art would not be motivated by the Nishimaki reference so

as to modify the Shibata reference to obtain the invention recited in new claims 16-32. Accordingly, it is respectfully submitted that new claims 16-32 and the claims that depend therefrom are clearly patentable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. However, if the Examiner should have any comments or suggestions to help speed the prosecution of this application, the Examiner is requested to contact the Applicant's undersigned representative.

Respectfully submitted,

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